Amendments to the Specification:

Please replace the Abstract beginning at page 42, line 2, with the following rewritten paragraph:

An ~~processor with a generalized~~ eventpoint chaining apparatus for generalized event detection and action specification in a processing environment ~~architecture, which is scalable for use in a very long instruction word (VLIW) array processor, such as the manifold array (ManArray) processor~~ is described. In one aspect, ~~generalized processor event (p-event) detection facilities are provided by use of compares to check if an instruction address, a data memory address, an instruction, a data value, arithmetic condition flags, or other processor change of state eventpoint has occurred. In another aspect, generalized processor action (p-action) facilities are provided to cause a change in the program flow by loading the program counter with a new instruction address, generate an interrupt, signal a semaphore, log or count the p-event, time stamp the event, initiate a background operation, or to cause other p-actions to occur. The generalized facilities are defined in the eventpoint architecture as consisting of a control register and three eventpoint parameters, namely at least one register to compare against, a register containing a second compare register, a vector address, or parameter to be passed, and a count or mask register. Based upon this generalized eventpoint architecture, new capabilities are enabled. For example, auto-looping with capabilities to branch out of a nested auto-loop upon detection of a specified condition, background DMA facilities, the ability to link a chain of p-events together for debug purposes, and others are all important capabilities which are readily obtained.~~ the eventpoint chaining apparatus includes a first processor which has a programmable

eventpoint module with an input trigger (InTrig) input. The first processing element detects an occurrence of a first processor event (p-event) and produces an OutTrigger (OT) signal. The eventpoint chaining apparatus also includes a second processor which has a programmable eventpoint module with an input trigger (InTrig) input which receives the OT signal from the first processing element. The second processing element detects an occurrence of a second p-event and produces, in response to the OT signal received from the first processing element and the detection of a second p-event, an eventpoint (EP) interrupt signal. The eventpoint chaining apparatus also includes a sequence processor interrupt control unit for receiving the EP interrupt signals indicating the occurrence of both the first and second p-events and causing a p-action in response to the occurrence of both the first and second p-events